CLAIMS

1. A scanning circuit, comprising:

a power supply providing a negative voltage on a first terminal, an intermediate voltage on a second terminal and a positive voltage on a terminal of a switch, the other terminal of the switch being connected to a third terminal,

a control circuit supplied by connections to the second and third terminals,

a differential amplifier receiving a positive and a negative input signal provided by the control circuit,

a power amplifier controlled by the differential amplifier, both amplifiers being supplied by connections to the first and third terminals,

a deflection coil connected between the output of the power amplifier and the second terminal,

biasing means setting, when the switch is open, the output of the differential amplifier so that the possible current paths through the power amplifier between the deflection coil and the first terminal are cut.

2. A scanning circuit according to claim 1, wherein the differential amplifier comprises eight transistors, the third and fourth transistors being of NPN type, the other transistors of PNP type, the base of the first transistor receiving the negative input signal, the base of the second transistor receiving the positive input signal, the emitters of the first and second transistors being connected to the collector of the sixth transistor, the emitter of the sixth transistor being connected to the third terminal, the base of the sixth transistor being connected to the collector of the eighth transistor, the base of the eighth transistor being connected to its collector, the emitter of the eighth transistor being connected to the third terminal, the collector of the eighth transistor being connected to a current source, the collector of the first transistor being linked to the first terminal by a first resistor, the collector of the second transistor being linked to the first terminal by a second resistor, the bases of the fifth and seventh transistors being connected to the base of the sixth transistor, the emitters of the fifth and seventh transistors being connected to the third terminal, the collector of the fifth transistor being connected to the collector of the third transistor,

the emitter of the third transistor being connected to the collector of the first transistor, the collector of the third transistor being connected to its base, the collector of the seventh transistor being connected to the collector of the fourth transistor, the emitter of the fourth transistor being connected to the collector of the second transistor, the base of the fourth transistor being connected to the base of the third transistor.

3. A scanning circuit according to claim 2, wherein a comparator receives on a first input a fixed voltage equal to the voltage of third terminal minus the voltage of a reference supply, the other input of the comparator being connected to the collector of the sixth transistor, a reference current source controlled by the comparator being connected to the collector of the third transistor.

4. A scanning circuit according to claim 2, wherein an auxiliary P-type zone is provided near the P-type zone forming the collector of the sixth transistor, the auxiliary P-type zone being connected to the collector of the third transistor.

5. A scanning circuit according to claim 2, wherein a P-type zone forms the common emitters of the fifth, sixth and seventh transistors, a N-type zone surrounding the emitter forms the common base of the transistors, three P-type zones surrounding the common base form the collectors of the transistors, all collectors being separated by narrow N-type zones, the length of opposite outlines of the collectors of the fifth and sixth transistors being larger than the length of opposite outlines of the collectors of the seventh and sixth transistors.

6. A scanning circuit according to claim 1, wherein the differential amplifier comprises an input transistor pair receiving the positive and the negative input signals, the input transistor pair forming a first amplifying stage coupled to a second amplifying stage, and wherein the sizes of the transistors of the input transistor pair are different and wherein the sizes of the components of the second amplifying

stage are different to balance the transistor size difference of the input transistor pair when the switch is open.